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Developers Conference

NuBus Development Strategies

NuBus Interface Solutions

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Agenda

- NuBus Milestones
- NuBus Interfaces
- TI NuBus Products
- Specific vs. General Solutions
- Documentation/Availability/Pricing
- The Future of NuBus

NuBus Milestones

- 1979   NuBus developed at MIT
- 1983   Texas Instruments acquires NuBus
- 1985   NuBus based Explorer Workstation
- 1987   NuBus based Macintosh II
- 1988   General purpose Chipset
- 1990   IEEE Revision Committee

NuBus Interfaces

- ## Simple Slave
  - Responds to Read/Write Transactions

- ## Master
  - Initiates Transactions, Reading/Writing to a Slave
  - Requires Arbitration Logic to Acquire Bus

- ## Master/Slave
  - Initiate & Respond to Transactions
  - Requires Slave & Master Logic

General Purpose Chipset

ACT2440/BCT2420/ALS2442

- Support Macintosh II NuBus
- Flexible - Master and/or Slave
- Cost Effective

Device Features

- Three Chip Solution

    - ACT2440 NuBus Controller

    - BCT2420 NuBus Transceiver (2 required)

- Address / Data Path Separate from Controller

    - Allows PAL-based controller for slave applications

- Packaged in 68 Pin PLCCs
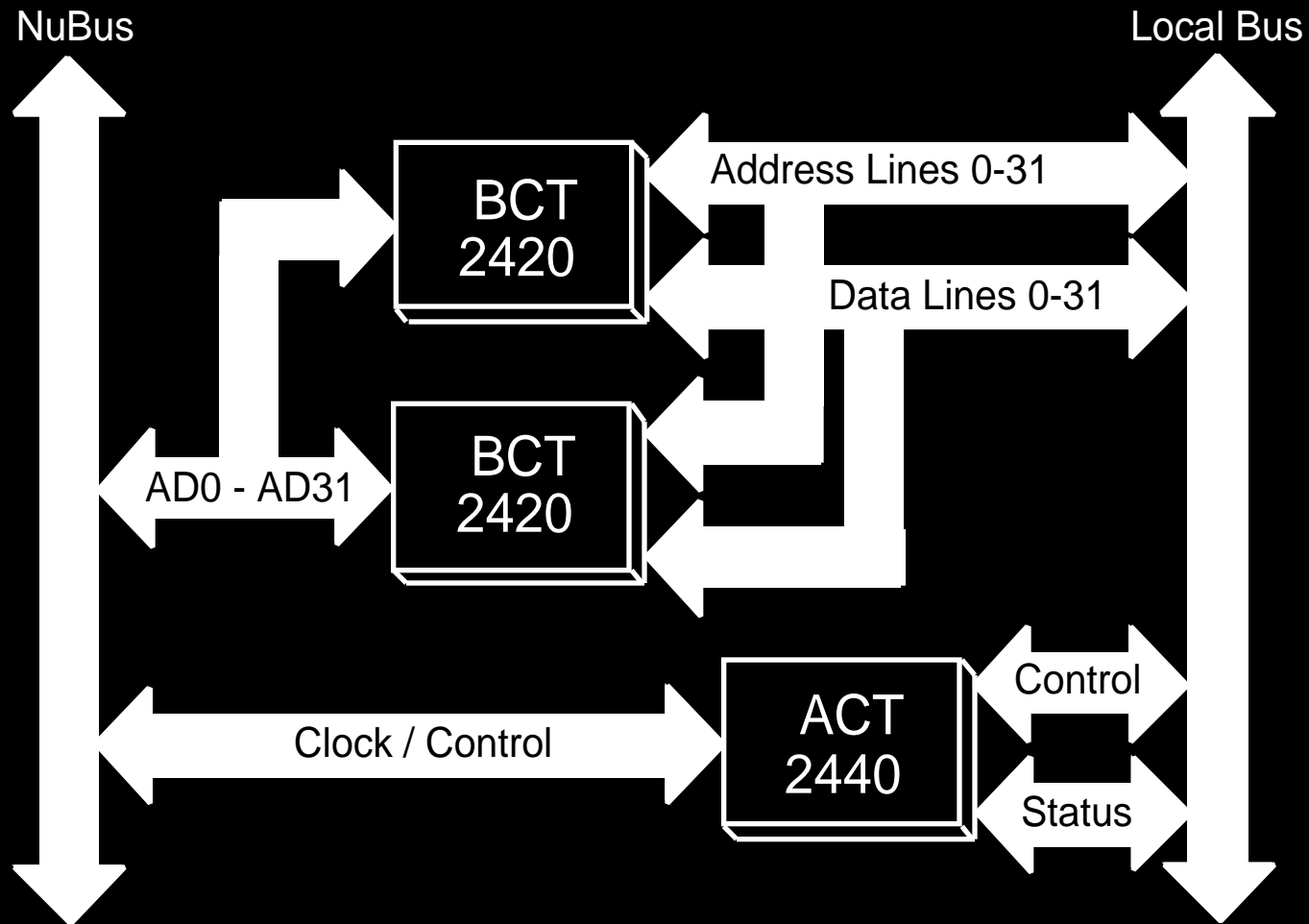
ACT2440

NuBus Controller

- Master, Slave, and Master / Slave Applications

- Direct NuBus Interface without external buffers

- Resource Locking

- Block Transfers with addition of ALS2442

BCT2420

NuBus Transceiver

- Three 16-bit I/O Ports

- On-chip comparator for slot identification

- BiCmos design for 24 ma drive/low power dissipation

General Purpose Chipset

NuBus

Local Bus

BCT 2420

Address Lines 0-31

Data Lines 0-31

AD0 - AD31

BCT 2420

ACT 2440

Control

Clock / Control

Status

Macintosh Coprocessor Platform Chipset

ACT2441/BCT2425

- Integrated Solution

- Reduced Board Space

- Lower Power Consumption

- 100 Pin Quad Flat Packages
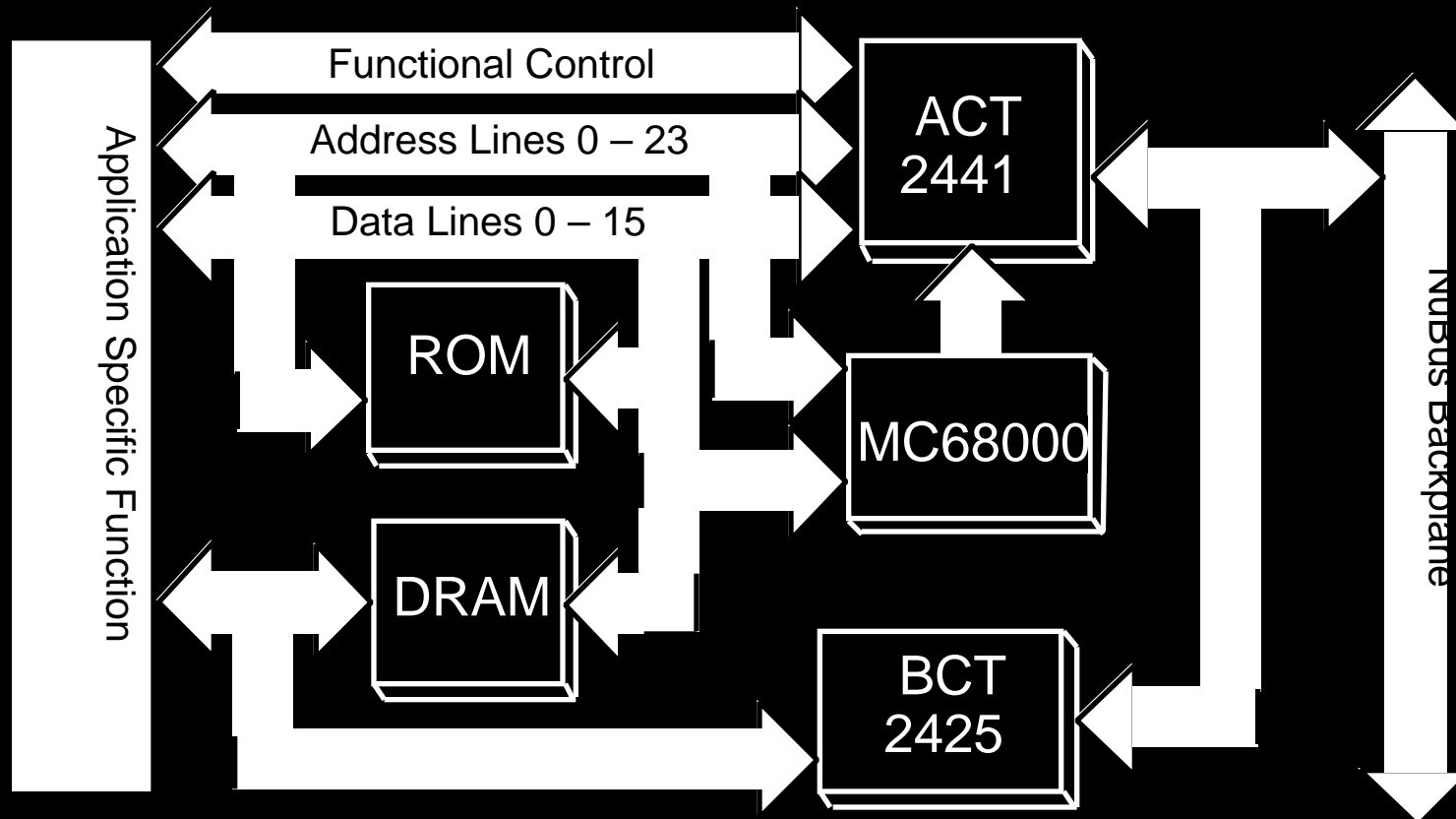
ACT2441

MCP Controller

- Interface to NuBus, DRAM, and MC68000

- Supplies DRAM Refresh

- Interface to Application Specific Processor

BCT2425

MCP Data Path Transceiver

- Interface to ACT2441

- Includes Memory Drivers

- BiCmos design for 24 ma drive/low power dissipation

MCP Chipset

Discrete vs. Integrated Solution

Feature	Integrated	Discrete
Chip Count	2 100-PIN QFPs	24 Devices
Board Area	1.62 sq. inches	SM 4.12 sq. inches DIP 6.87 sq. inches
Power	.38 Watts	7.37 Watts

Specific vs. General Solution

- MCP Benefits
    - A/ROSE Software
    - MC 68000 Integration
- General Purpose Chipset Benefits
    - Processor Independence
    - Higher Transfer Performance Potential
    - Configurable to Application

Availability & Pricing

Pricing

1000 Unit Volumes

Databook & Samples
Available

ACT2440	$15.15
BCT2420	$6.50
ALS2442	$4.90
ACT2441	$27.00
BCT2425	$16.20

Solution Cost

NuBus Interface	Unit Cost
Slave Only (2 x BCT2420's)	$13.00*
Master/Slave (ACT2440 + 2 x BCT2420)	$28.15
MCP (ACT2441, BCT2425)	$43.20

* Requires PAL Controller

NuBus Futures

- IEEE Committee (P1196-R)

- Enhanced Burst Mode Feature
  - 71 Mbytes/sec

- Other Issues
  - Cached Coherency Protocol
  - Standby Power
  - Support for P1394 Serial Bus

For Information, Contact:

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Secretary, P1196-R

Apple Computer

AppleLink ATWOODJ

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NuBus Development Strategies

A/ROSE™ Software Development

David Comstock

Senior Software Engineer

Apple Computer, Inc

A Brief History of A/ROSE™

- Originally called MR-DOS
- Developed for Internal Projects / Developers
- First Official Release – Summer 1989
- Available from APDA

Macintosh Coprocessor Platform™

- Motorola 68000 – 10 MHz
- 512K – 1MB RAM
- 4 MB Address Space
- 35 Sq. Inches of Prototyping Area

Main Components of A/ROSE

- A/ROSE

  - Operating System for NuBus Cards

  - 680xx Processor

  - NuBus Master

- A/ROSE Prep Driver

  - Motherboard Driver

  - Provides A/ROSE Services to Macintosh O/S

Key A/ROSE Features

- Task Scheduling

- Memory Management

- Inter-process Communication

- Naming Services

A/ROSE Specifications

- 256 Tasks per Card

- 32 Priority Levels

- 512 Message Buffers/Card (Default)

A/ROSE Memory Usage

- Full Configuration
  - 23K + Buffers

- Minimal Configuration
  - 6K + Buffers

- Buffers
  - 48K (Default)

A/ROSE Performance

- 110 μsec Context Switch Time

- 20 μsec Interrupt Latency

- > 1,000 Messages per Second (Inter-card)

- > 3,400 Messages per Second (Intra-card)

- > 1,400 Messages per Second (Mac – Card)

Why use A/ROSE?

- Flexibility

  - Real Time / Multi-tasking

  - High Performance / Small Size

  - Dynamically Downloaded Tasks

- Reduced Time to Market

  - Low-Level NuBus Interface Provided

Apple's Commitment

- Existing and Future NuBus Cards / Software

- Compatibility

  - New Macintoshes / System Software

- Other Developments

Utilities

- Dumping

- Tracing

- Downloading

- Displaying messages

- Debugger

NuBug

- Debugger for NuBus Cards

- Looks and Acts like MacsBug

- A Resizable Window for Each Card Running A/ROSE

- MultiFinder Friendly

Slot B

Slot C

```
A7
00000000
```

```
00 FB100000
04 FB0074A2
08 FB002B98
0C FB002BA4
10 FB002BB0
14 FB002BBC
18 FB002BC8
1C FB002BD4
20 FB002BE0
24 FB002BEC
28 FB002BF8
```

```
        A7
    FC07FF7C
7C  FC003214
80  0004FC00
84  237E0000
88  FC00213A
8C  00000008
90  00000013
94  00000000
98  00000000
9C  00000000
A0  00000000
A4  00000000

    SR    Int
  SxNzvc   0

D0  FC07EF50
D1  00000001
D2  0000002C
D3  00000000
D4  00000000
D5  0000034D
D6  0000FFFF
D7  0000000B

A0  FC073D38
A1  FC07EF50
A2  FC077860
A3  FC073D38
A4  FC000BB2
A5  FC001D3A
A6  FC07EA58
A7  FC07FF7C
US  FC07EA94
PC  FC0035A2
```

```
Return shows the sections sequentially.
 HELP name or ? name shows that section
  The following topics are available
    Assemble
    Breakpoints
    Disassembly
    Editing
    Expressions
    Find
    Go
    Load
    Memory
    Miscellaneous
    Registers
    Stack
    Step
    Symbol
Breakpoints
 BR addr [n]
    Break at addr after n times. If n is not specified then break always
 BRC [addr]
    Clear breakpoint at addr or all breakpoints if no addr
 BRD
    Display breakpoint table
Processor halted at FC0035A2
```

```
main+17CC
  FC0035A2 *MOVEA.L    $0004(A1),A0                        | 2069 0004
```

B: Running

C: Stopped

Trash

Documentation

- Full Manual

- Source Code Examples

- Schematics for MCP Prototyping Card

Developer Technical Support

- AppleLink: MACDTS

Distribution / Pricing

- Available from APDA

- Macintosh Coprocessor Platform Kit
  - Prototyping Card, Software, Documentation
  - M0793LL/A $500

- MCP Documentation
  - M0301LL/B $65

A/ROSE Limitations

- Provides Basic Services

    - Memory Mangement, but No Memory Protection

- Not Optimized for Specific Applications

    - No Burst Mode Support

- No Support for Bus Slave Cards

A/ROSE Futures

- A/UX 2.0 Support

- Portable C Version

- PPC Interface

- 68030 NuBus Card Support

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